Wei Ye

Education

University of Texas at Austin — **Austin, TX**
Ph.D., Electrical and Computer Engineering, GPA: 3.87/4.00 — *Aug 2015 – May 2020*
Advisor: David Z. Pan

Zhejiang University — **Zhejiang, China**
B.Eng., Electronic and Information Engineering, GPA: 3.96/4.00 — *Sep 2011 – Jun 2015*

Professional Experience

Kioxia (Toshiba Memory Corporation) — **Yokohama, Japan**
Research Intern, **Deep learning for computational lithography** — *Jun 2019 – Aug 2019*
- Designed generative adversarial network (GAN) models for approximating time-consuming lithography simulation
- Achieved high accuracy on advanced benchmarks and 1000× speedup compared with conventional simulation tool

Cadence Design Systems — **Austin, TX**
Software Intern, **Network programming for software communication** — *May 2018 – Aug 2018*
- Designed and implemented socket communication and co-simulation framework between Cadence Voltus and Cadence Spectre with C++ Boost Asio library

Synopsys Inc. — **Sunnyvale, CA**
Technical Intern, **Algorithm design for reliable circuits** — *May 2016 – Aug 2016*
- Designed and implemented algorithms for on-the-fly detection of design rule violations in clock tree synthesis
- Verified on commercial benchmarks and achieved improvement of slack estimation by 37% and final design quality

Research Experience

Machine Learning and Its Applications in VLSI CAD, UT Austin — *May 2018 – Present*
- Designed various GAN models to substitute time-consuming lithography simulation [DAC'19, ISPD'20]
- Developed lithography hotspot detection flow with active learning and Gaussian process regression [DATE'19]
- Developed electromigration hotspot detection and fixing methods with multistage logistic regression [ASPDAC'19]

Algorithm Design for VLSI Physical Design Automation, UT Austin — *Sep 2015 – May 2018*
- Developed scalable power grid reduction algorithm with convex optimization method [ISPD'18]
- Designed and implemented placement algorithms for improving circuit reliability [ISLPED'17]

Publications

Book Chapter

[B1] **Wei Ye**, Mohamed Baker Alawieh, Che-Lun Hsu, Yibo Lin, and David Z. Pan, "Dealing with Aging and Yield in Scaled Technologies", In: Dependable Embedded Systems. Springer, 2019

Journal Articles

[J1] Mohamed Baker Alawieh, Yibo Lin, **Wei Ye**, and David Z. Pan, "Generative Learning in VLSI Design for Manufacturability: Current Status and Future Directions", Journal of Microelectronic Manufacturing (JOMM), 2019

Conference Papers

[C9] **Wei Ye**, Mohamed Baker Alawieh, Yuki Watanabe, Nojima Shigeki, Yibo Lin, and David Z. Pan, "TEMPO: Fast Mask Topography Effect Modeling with Deep Learning", ACM International Symposium on Physical Design (ISPD), 2020 (Best Paper Finalist)

[C8] **Wei Ye**, Mohamed Baker Alawieh, Yibo Lin, and David Z. Pan, "LithoGAN: End-to-End Lithography Modeling with Generative Adversarial Networks", ACM/IEEE Design Automation Conference (DAC), 2019 (Best Paper Finalist)

[C7] **Wei Ye**, Mohamed Baker Alawieh, Meng Li, Yibo Lin, and David Z. Pan, "Litho-GPA: Gaussian Process Assurance for Lithography Hotspot Detection", IEEE Design, Automation & Test in Europe Conference & Exhibition (DATE), 2019

[C6] **Wei Ye**, Yibo Lin, Meng Li, Qiang Liu, and David Z. Pan, "LithoROC: Lithography Hotspot Detection with Explicit ROC Optimization", IEEE/ACM Asian and South Pacific Design Automation Conference (ASPDAC), 2019

[C5] **Wei Ye**, Mohamed Baker Alawieh, Yibo Lin, and David Z. Pan, "Tackling Signal Electromigration with Learning-Based Detection and Multistage Mitigation", IEEE/ACM Asian and South Pacific Design Automation Conference (ASPDAC), 2019

[C4] Yibo Lin, Mohamed Baker Alawieh, **Wei Ye**, and David Z. Pan, "Machine Learning for Yield Learning and Optimization", IEEE International Testing Conference (ITC), 2018 (Invited)

[C3] **Wei Ye**, Meng Li, Kai Zhong, Bei Yu, and David Z. Pan, "Power Grid Reduction by Sparse Convex Optimization", ACM International Symposium on Physical Design (ISPD), 2018

[C2] **Wei Ye**, Yibo Lin, Xiaoqing Xu, Wuxi Li, Yiwei Fu, Yongsheng Sun, Canhui Zhan, and David Z. Pan,"Placement Mitigation Techniques for Power Grid Electromigration", IEEE International Symposium on Low Power Electronics and Design (ISLPED), 2017

[C1] **Wei Ye**, Bei Yu, Yong-Chan Ban, Lars Liebmann, and David Z. Pan, "Standard Cell Layout Regularity and Pin Access Optimization Considering Middle-of-Line", ACM Great Lakes Symposium on VLSI (GLSVLSI), 2015

Skills

Languages: C/C++, Python (Tensorflow, PyTorch), Verilog, MATLAB, Bash, LaTeX

Tools: Boost C++ Libraries; Intel MKL library; Gurobi Solver; Hypergraph partitioning package (hMETIS)

Courses

Engineering Programming Languages, Large Scale Optimization, Numerical Analysis: Linear Algebra, Data Mining, Multicore Computing, High-Speed Computer Arithmetic

Selected Awards

2015–2019: UT Graduate Student Fellowship — *University of Texas at Austin*

2018: Cadence Women in Technology Scholarship — *Cadence Design System*

2012,2014: National Scholarship — *Ministry of Education, P. R. China*

2013: Samsung Scholarship — *Zhejiang University*